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1. A co-simulation system for design verification of an electronic circuit, comprising:

a high-level modeling system (HLMS);

wherein the HLMS is a software tool executable on a computing arrangement;

a boundary-scan interface coupled to the high-level modeling system and configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol;

a re-configurable hardware platform coupled to the boundary-scan interface;

a translator coupled to the boundary-scan interface, implemented on the re-configurable hardware platform, and configured to translate input signals compliant with the boundary-scan protocol to signals compliant with a second protocol;

a first component instantiated within a wrapper component, wherein the wrapper component is coupled to the translator and is configured to transfer input signals of the second protocol to the first component; and

a second component co-simulated by the HLMS in software while the first component is co-simulated on the reconfigurable hardware platform;

wherein the HLMS-issued commands include at least one command that forces input co-simulation data from the second component to the first component, and/or at least one command that extracts output co-simulation data from the first component for input to the second component.

2. The system of claim 1, wherein the wrapper component further includes a memory map.

3. The system of claim 2, wherein the memory map includes a first set of registers for data input to the first component and a second set of registers for data output from the component.

4. The system of claim 1, wherein the translator includes a shift register, input data is serially shifted into the register and output in parallel to the first component, and output data is input in parallel in the shift register and serially shifted out.

5. A system for interfacing a high-level modeling system (HLMS) with a hardware platform for co-simulation of a first component on the hardware platform for design verification of an electronic circuit, comprising:

an interface coupled to the HLMS and configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol, and translate signals compliant with the boundary-scan protocol to data compatible with the HLMS;

wherein the HLMS is a software tool executable on a computing arrangement;

wherein the HLMS-issued commands include at least one command that forces input co-simulation data from a second component to the first component, and/or at least one command that extracts output co-simulation data from the first component for input to the second component;

wherein the second component is co-simulated by the HLMS in software while the first component is co-simulated on a reconfigurable hardware platform;

a translator coupled to the interface, implemented on the re-configurable hardware platform, and configured to translate input signals compliant with the boundary-scan protocol to signals compliant with a second protocol, and translate output signals compliant with the second protocol to signals compliant with the boundary-scan protocol; and

a wrapper component implemented on the re-configurable hardware platform, the wrapper component coupled to the translator and being configured for instantiation of the first component within the wrapper component and configured to transfer input signals of the second protocol to the first component and transfer output signals of the second protocol to the translator.

6. The system of claim 5, wherein the wrapper component further includes a memory map circuit coupled to an address decoder circuit.

7. The system of claim 6, wherein the memory map circuit includes a first set of registers for data input to the first component and a second set of registers for data output from the first component.

8. The system of claim 5, wherein the translator includes a shift register, input data is serially shifted into the shift register and output in parallel to the first component, and output data is input in parallel in the register and serially shifted out.

9. A method for interfacing a high-level modeling system (HLMS) with a reconfigurable hardware platform for design verification of an electronic circuit, comprising:

co-simulating a first component on the reconfigurable hardware platform in hardware while co-simulating a second component on the HLMS;

wherein the HLMS is a software tool executable on a computing arrangement;

coupling an interface to the HLMS, wherein the interface is configured to translate signals compliant with a boundary-scan protocol to data compatible with the HLMS;

wherein the interface further translates HLMS-issued commands to signals compliant with the boundary-scan protocol, and the HLMS-issued commands include at least one command that forces input co-simulation data from the second component to the first component, and/or at least one command that extracts output co-simulation data from the first component for input to the second component;

configuring the reconfigurable hardware platform with a translator and a wrapper component coupled to the translator; and

coupling the translator to the interface, wherein the translator is configured to translate signals compliant with a second protocol to signals compliant with the boundary-scan protocol;

wherein the wrapper component is configured for instantiation of the first component within the wrapper component and configured to transfer signals of the second protocol to the translator.

10. The method of claim 9, further comprising mapping data input to the first component and data output from the first component to an addressable memory space.

11. The method of claim 10, wherein the addressable memory space includes a first set of registers for data input to the first component and a second set of registers for data output from the first component.

12. The method of claim 9, further comprising serially shifting input data into a register and outputting in parallel data from the register to the first component, and storing output data from the first component in parallel in the register and serially shifting output data from the register to the boundary scan interface.

13. An apparatus for interfacing a high-level modeling system (HLMS) with a reconfigurable hardware platform for design verification of an electronic circuit, comprising:

means for co-simulating a first component on the reconfigurable hardware platform in hardware while co-simulating a second component on the HLMS;

wherein the HLMS is a software tool executable on a computing arrangement;

means for coupling a boundary-scan interface to the HLMS, wherein the boundary-scan interface is configured to translate HLMS-issued commands to signals compliant with a boundary-scan protocol, and translate signals compliant with the boundary-scan protocol to data compatible with the HLMS;

wherein the HLMS-issued commands include at least one command that forces input co-simulation data from the second component to the first component, and/or at least one command that extracts output co-simulation data from the first component for input to the second component;

means for configuring the reconfigurable hardware platform with a translator and a wrapper component coupled to the translator;

means for coupling the translator to the boundary-scan interface, wherein the translator is configured to translate input signals compliant with the boundary-scan protocol to signals compliant with a second protocol, and translate output signals compliant with the second protocol to signals compliant with the boundary-scan protocol; and

means for configuring the wrapper component to instantiate the first component within the wrapper component, and means for transferring input signals of the second protocol to the first component and for transferring output signals of the second protocol to the translator.